Research Inventy: International Journal of Engineering And Science
Vol.4, Issue 8 (August 2014), PP 70-73
Issn (e): 2278-4721, Issn (p):2319-6483, www.researchinventy.com

Circuit for Square Root of Multiplication

K.C.Selvam
Department of Electrical Engineering Indian Institute of Technology, Madras
Chennai – 600 036, India

ABSTRACT: *A circuit which accepts two input dc voltages V_I, V_2 and produces an output voltage $V_O = \sqrt{V_I V_2}$ by using double dual slope principle with op-amps and analog switches is described in this paper. Verification of the feasibility of the circuit is established by way of test results on a proto type.*

KEY WORDS: *Integrator, flip flop, comparator, transistor switch and peak detector*

I. INTRODUCTION

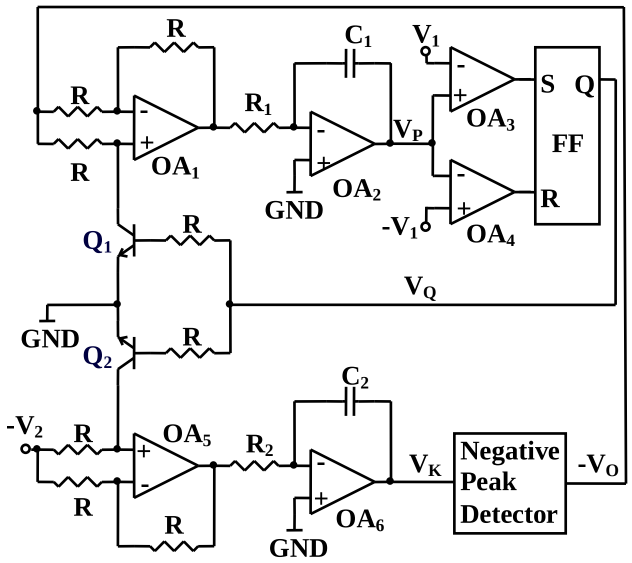
Square rooters find applications in many measurement and instrumentation system. Few examples are (i) Phase sensitive detector and (ii) Impedance measurement. The author Selvam proposed few square rooters by using (i) double dual slope integrators, double control amplifiers, one comparator and one peak detector [1] (ii) a saw tooth generator, comparator, switch and two op-amps [2] and (iii) a square rooter in which a multiplier is used in the feedback path of an operational amplifier (OP-AMP) [3]. There are several other square rooting circuits. (i) Rievuraja and Kamsri realised a technique [4] by use of the op-amp supply current sensing which utilises an inherently quadratic characteristic of the op-amp class –AB output stage. (ii) Rievuraja propsed a square rooter [5] using operational transconductance amplifiers (OTAs) as the only active elements. (iii) Filanovsky and Balkes proposed a square rooter [6] by using an opamp and two nested transistors. One of these transistors is in pinch – off and the other in the triode region of operation. (iv) Liu's square rooter [7] in which second generation current conveyors is used as high performance active building block. A further extension of square rooter circuit is the square root of multiplication of two voltages. Double dual slope multiplier – cum- divider circuit proposed by the author in [8] is reformatted to function as square rooting of multiplication and is explained in this letter.

II. CIRCUIT ANALYSIS

The proposed circuit diagram is shown in the Fig. 1. Let initially, the SR flip flop output be LOW (-V_{CC}). The transistor Q_1 is OFF, control amplifier OA_1 will work as non-inverting amplifier and hence the integrator OA_2 output will be

$$V_P = \frac{1}{R_1 C_1}\int_0^{t1} V_O\, dt + V_P(0) = \frac{V_O}{R_1 C_1} t1 + V_P(0) \qquad (1)$$

When the output of the integrator OA_2 exceeds the second input voltage V_1, say at time t_1, the SR flip flop is set to HIGH (+V_{CC}) by comparator OA_3. The transistor Q_1 is ON, control amplifier OA_1 will work as inverting amplifier and hence the integrator output will then be



Fig, 1 Proposed circuit diagram of square root of multiplication

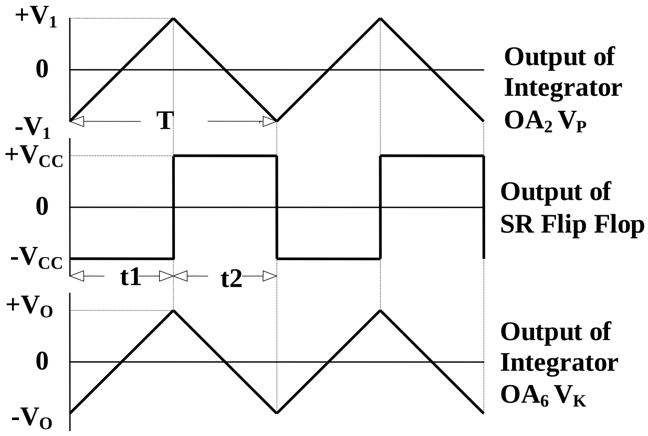


Fig.2 Associated waveforms of Fig. 1

$$V_P = \frac{1}{R_1 C_1}\int_{t1}^{t} -V_O\,dt + V_P(0) = -\frac{V_O}{R_1 C_1}(t - t1) + V_P(0) \qquad (2)$$

When the output of the integrator exceeds the second input voltage $-V_1$, say at time t_1+t_2, the RS flip flop is reset to LOW by the comparator OA_4 and the cycle repeats. The associated waveforms generated under steady state operation are shown in Fig. 2, where $V_P(0)$ is taken as $-V_1$. From equation (1) and referring to fig we have under steady state condition, $t_1 = t_2 = T/2$ and at t, $V_P = 2V_1$ and hence

$$2V_1 = \frac{V_O}{R_1 C_1}\frac{T}{2} \qquad (3)$$

$$T = \frac{4V_1 R_1 C_1}{V_O} \qquad (4)$$

The ON time of the square waveform V_Q at the output of SR Flip Flop shorts the non-inverting terminal of op-amp OA_5 to GND through the transistor Q_2. The amplifier OA_5 will work as inverter and V_2 is connected to the integrator OA_6. Its output V_K will be

$$V_K = \frac{1}{R_2C_2}\int -V_2 dt = -\frac{V_2}{R_2C_2}t \qquad (5)$$

The OFF time of V_Q will enable the amplifier OA_5 to work as non-inverting amplifier and hence $-V_2$ will be given to the integrator OA_6. Then its output will be

$$V_K = \frac{1}{R_2C_2}\int V_2 dt = \frac{V_2}{R_2C_2}t \qquad (6)$$

Another triangular wave of peak to peak value of $\pm V_O$ is generated at the output of OA_6. From Equation (6) and waveforms in Fig. 2, the fact that at t=T/2, $V_K = 2Vo$

$$2V_O = \frac{V_2}{R_2C_2}\frac{T}{2} \qquad (7)$$

$$V_O = \frac{V_1V_2}{V_O}\frac{R_1C_1}{R_2C_2} \qquad (8)$$

If $R_1C_1 = R_2C_2$, then

$$V_O{}^2 = V_1V_2 \qquad (9)$$

$$V_O = \sqrt{V_1V_2} \qquad (10)$$

III. EXPERIMENTAL RESULTS AND CONCLUSION

The proposed circuit is tested in our laboratory. LF 356 ICs are used for all op-amps. IC 4027 is used for SR Flip-Flop. Conventional peak detector circuit using op-amp is used. A power supply of $\pm V_{CC} = \pm 7.5V$ is chosen. The test results are shown in graphs of Fig. 3 and Fig. 4. A new circuit for square rooting of multiplication is described. The polarity of all input voltages must be single polarity only. Hence the proposed circuit is of single quadrant type.

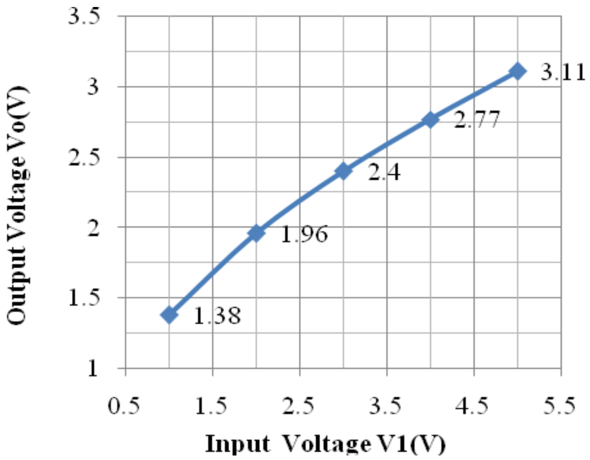


Fig. 3 Test results for constant V_2 = 2V

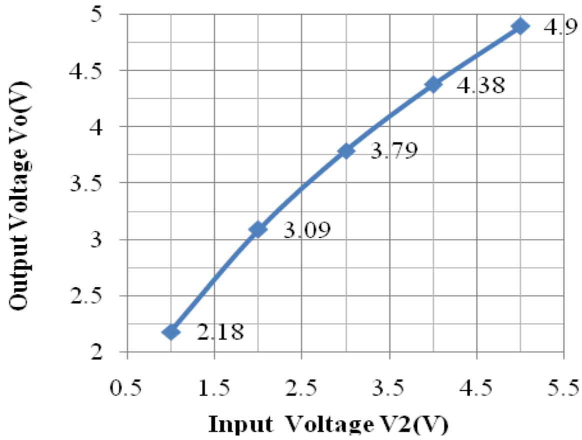


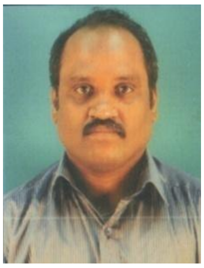
Fig. 4 Test results for constant V_1 = 5V

IV. ACKNOWLEDGEMENT

The author is highly indebted to his loving wife Mrs. S. Latha for circuit drawing, waveforms drawing, discussions and proof readings. He also thanks Prof. Dr. S. Srinivasan, Prof. Dr. V.Jagadeesh Kumar, Prof. Dr.Sridharan, Dr. Arun Mahindrakar, Dr. Bharath Bhikkaji and Dr. Ramakrishna Pasumarthy, Department of Electrical Engineering, Indian Institute of Technology, Madras, for their encouragement throughout the work.

REFERENCES

[1] K.C. Selvam, "Double dual slope square rooter," IET The Journal of Engineering, Doi: 10.1049/joe.2013.0225, January 2014
[2] K.C.Selvam, "Square rooter using saw tooth wave – based time division technique," IET The Journal of Engineering, doi:10.1049/joe.2013.0259, February 2014
[3] K.C.Selvam and S.Latha, "A simple square rooting circuit based on operational amplifiers", Engineering, Technology & Applied Science Research, Vol.3, No. 1, pp: 349-351, 2013
[4] V. Rievuraja and T. Kamsri, "Square-rooting and absolete function circuits using operational amplifiers", IET Circuits, Devices & Systems, Vol.3, Issue 2, pp: 57-63, 2009
[5] V. Riewuraja, "A simple square rooting circuit using OTAs", Electronic Letters, Vol.44, Issue 17, pp: 1000-1002, 2008
[6] I.M. Filanovsky and H.P. Balkes, "A simple CMOS analog square – rooting and squaring circuits" IEEE Trans on circuits and systems I, Fundamental theory and applications, Vol.39, Issue:4, pp:312-315, 1992
[7] S.I.Liu, "Square-rooting and vector summation circuits using Current conveyors," IEE Proc.Circuits., Dev.Syst., Vol.142, pp 223-226, 1995.
[8] K.C.Selvam, "Double dual slope multiplier – cum – divider" Electronics Letters, Vol.49, No.23 pp: 1435-1436, 7th November 2013.



K.C. Selvam was born on 2nd April 1968 in Krishnagiri District of Tamil Nadu State, India. He was graduated by the Institution of Electronics and Telecommunication Engineers, New Delhi, in the year 1994. He has published 23 research papers in various national and international journals. He got best paper award by IETE in the year 1996. At present he is working as Technical Staff in the Department of Electrical Engineering, Indian Institute of Technology, Madras, India. He developed interest in design and development of function circuits to find their applications in modern measurements and instrumentation systems.