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A Novel DC-DC Converter for Photo Voltaic Application

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ABSTRACT: *This work presents a sub-module power management system for large-scale photovoltaic systems. Individual 'micro-converters' configure across strings of PV cells at terminals normally connected to bypass diodes. The converters enforce set voltage ratios among adjacent strings of cells, mitigating power loss due to shading, factory and lifetime variation, and other sources of mismatch. The balancing function extends to multiple series-connected PV modules through a dual-core cable and connector, enabling high-voltage operation with active and passive components exposed to only a fraction of total system voltage. Converters are based on a resonant switched-capacitor standard switching cell. The module-integrated converter achieves conversion efficiency over 99% for a wide range of mismatch scenarios and insertion loss below 0.1 %.*

KEY WORDS: *switched capacitor, photovoltaic energy, DC-DC maximum power point tracking (MPPT).*

I. INTRODUCTION

Traditional photovoltaic (PV) modules are configured as strings of PV cells that operate as photo-diodes to capture energy from the sun. Shown in Fig. 1, cells are connected in series to minimize wiring and achieve sufficient voltage for DC-AC inverters to operate efficiently. While the series connection of cells is effective and necessary, it is problematic when PV cells are mismatched or regions of panels are shaded [1-3]. This problem is especially severe when large arrays are managed with only a single point of control (central inverter) [3-4]. Architectures based on distributed power electronics, such as work outlined in [4-6], have emerged to provide better control and higher energy capture in scenarios with cell mismatch due to shading, factory variation, aging, The traditional PV power management architecture is based on a central inverter that manages one or more series-connected strings of PV panels [1]. The central inverter implements a maximum power point tracking (MPPT) algorithm that optimizes power flow from the solar array. Problems arise when there is mismatch among PV panels or strings of PV cells.

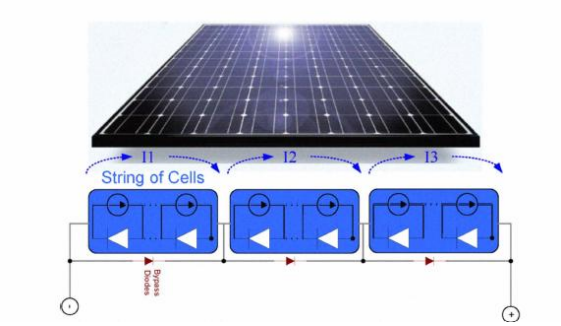

Fig. I. Typical PV module with 3 strings of cells

Mismatch can arise from many sources including direct shading, dust, debris, cell aging, and factory mismatch [2]–[6]. In a string of panels, all PV cells are connected in series such that the current must be equal in all cells. With mismatch, the current in the series string is limited to the worst case cell in the string. In a traditional array, there may be ten or more panels connected in series which can result in hundreds of series-connected PV cells.

Bypass diodes placed in parallel with strings of cells in each PV module allow current to flow around underperforming strings of cells, but throw away energy produced by these cells and incur extra power loss in the diodes. This causes several problems: 1) power from underperforming cells can be lost even if it is only slightly lower than average, 2) the maximum power voltage *V*mpp in strings of panels with bypass diodes "ON" will not match the *V*mpp of other strings—resulting in power loss in all panels in the string, and 3) bypass diodes can cause discontinuities in the power–voltage curve for the array, complicating and potentially destabilizing the MPPT algorithm for the central inverter.In this work we present a power management architecture based on a distributed resonant-switched capacitor (ReSc) converter that leverages a 0.351lm HVCMOS IC to increase energy capture in real-world conditions that include shading and mismatch. The converter is designed to integrate into the junction box of conventional 225W crystalline-Si solar modules with open-circuit voltage up to 60V and short-circuit current in the range of 8A. The system is modular, such that it can extend to strings of modules of many tens of kW and be implemented in traditional architectures without reconfiguring the central inverter. Here we demonstrate the solution in a 2.7 kW PV array with an off-the-shelf central inverter. The proposed solution has advantages compared to traditional DC-DC MPPT solutions, achieving effective conversion efficiency over 99% and insertion loss below 0.1 % while balancing power flow at the sub-module level without rewiring solar modules. The rest of this paper is organized as follows. Section II describes the sub-module converter architecture and advantages compared to traditional implementations. Section III describes the resonant switched capacitor (ReSC) circuit implementation. Section IV discusses measurement results and comparison to theory.

$$\eta_{eff} = \frac{P_T - (1-\eta_C)P_\Delta}{P_T}, \qquad (1)$$

II. SUB - MODULE CONVERTER ARCHITECTURE

Fig. 1 shows a high-level representation of the proposed sub-module architecture. Distributed converters are configured in parallel with sub-module PV units – in this case, strings of PV cells that are normally in parallel with bypass diodes. Multiple series-connected converters operate together as a distributed ladder converter enforcing set voltage ratios among adjacent strings of cells. In the proposed implementation, converters enforce 1: 1 voltage ratios, equivalent to voltage equalization. The strategy enhances the MPPT algorithm of the central power-point tracking inverter: local converters enforce operation of each string of cells at sub-fractional maximum power voltage (V mpp), optimizing power production. The parallel configuration has several advantages compared to traditional DC-DC (buck-boost) converter implementations: 1) converters handle only mismatch power, 2) converters can 'tum off if there is no mismatch detected in the system, 3) active and passive components are exposed to only a fraction of total system voltage stress. Advantage 1) provides multiplication of effective conversion efficiency because the dominant power flow path remains in series through PV cells. For example, if individual converter stages operate with 90% efficiency for direct power flow, but handle only 10% of total power then effective conversion efficiency is 99%. This relation can be expressed as followswhere η eef is total effective conversion efficiency, ηc is conversion efficiency of the unit converter stage, P t; is mismatch power, and P T is total power produced by the PV cells. Advantage 2) enables significantly lower insertion loss compared to traditional DC-DC converter solutions.In this work, we define insertion loss as power loss overhead of distributed converters compared to the nominal (unshaded) power production of the PV array. For example, if PV modules are configured with DC-DC

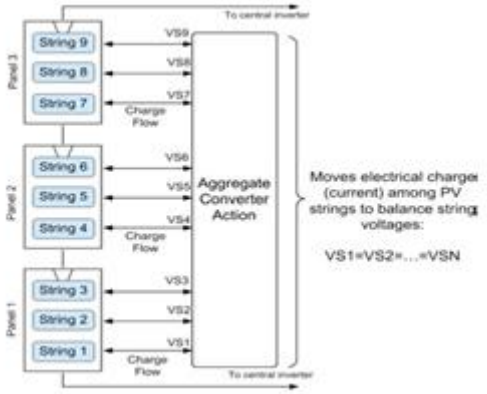

Fig. 2. Proposed resonant ladder converter architecture

converters that have nominal conversion efficiency of 98%, insertion loss includes the conversion efficiency penalty of 2%. In some examples DC-DC converters can operate in a pass-through or bypass mode when conversion ratio is 1:1 [5]. In this case, conversion efficiency of 99.5% or insertion loss of 0.5% has been reported [5, 8]. In practice this approach requires the central inverter to operate the PV array with the exact voltage such that unity conversion ratio is achieved. This may be complicated for an array with multiple parallel strings of PV modules: strings may have different optimum pass-through voltages, especially if there is shading in the array.Advantage 3) provides significant improvement in the overall power density of the converter – improving tradeoffs among size, weight, and conversion efficiency. It also enables the use of moderate voltage components that are widely available, such as ceramic capacitors and silicon-based MOSFETS. In-line with the discussion in [10-12], this is a core advantage of ladder-type converters including switched-capacitor topologies as compared to traditional buck-boost magnetic converters. The proposed architecture has a resemblance to known battery equalization architectures, [9], and module-level balancing architectures, [7]. The advantage of the proposed configuration compared to [7] is derived from advantage 3) above. The converter in [7] requires certain active and passive components to be exposed to the full system voltage stress. This limits the power density and conversion efficiency of the converter due to high DC bus voltages in typical grid-connected PV systems. The architecture also extends on the work in [9]. The difference here is the use of resonant conversion cells, significant improvement in the floating gate-drive circuit, and customization to the PV application space.
The architecture leverages the high conversion efficiency and reliability of state-of-the-art central inverters while providing a means to recover mismatch loss and implement other distributed control functions. As such it may be an attractive alternative in moderate to large-scale installations where micro-inverter cost
and performance are less compelling.

III. PROPOSED ARCHITECTURE

The proposed approach, shown in Figs. 2 and 3, is based on a distributed converter that is integrated in the junction box connector of each solar panel. In contrast with traditional dc – dc solutions that perform MPPT, the regulation objective of the proposed distributed converters is to enforce voltage ratios, not absolute voltages, among series-connected PV units. The converters interface across strings of cells in each panel in the traditional location of the bypass diodes, enabling better granularity of control than traditional dc–dc solutions. The distributed converters form an aggregate ladder converter that allows power to flow in parallel with the series-connected PV modules. Fig. 3 shows the aggregate converter for one string of modules. In typical PV modules, the voltage ratios of adjacent strings of cells are 1:1 assuming the strings have the same number of Cells of the same technology. Since cell voltage is logarithmic with current to first order, maximum power voltage *V*mpp is significantly less sensitive to mismatch than maximum power current *I*mpp. Fig. 4 shows a comparison of the normalized *I*mpp and *V*mpp versus short-circuit current *I*SC for a typical string of PV cells. *I*mpp is linear with

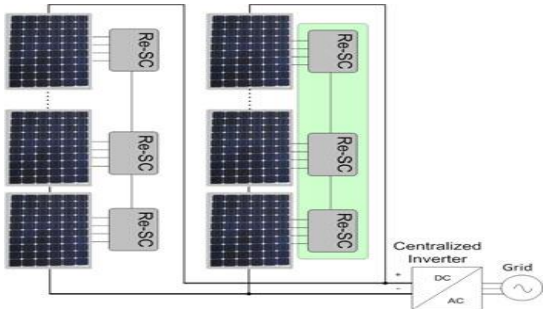

Fig. 3.Effective aggregate converter for one string of PV modules.

I_{SC} to first order, while *V*mpp stays within a narrow range for nearly a decade of variation of *I*SC. *V*mpp is logarithmic with *I*SC to first order, but has some higher order curvature due to series and shunt resistive effects. Maximum power voltage does have dependence on temperature such that thermal gradients can cause deviation from the 1:1 ratio, but the effect may only be a few percent even with thermal gradients up to 10–20 ◦C. Therefore, to first order, voltage equalization is effective to mitigate mismatch loss. In the example discussed here, the converter enforces voltage ratios of 1:1 between adjacent strings of cells, which is equivalent to voltage equalization [13]. In the proposed system, the central inverter finds the maximum power voltage for the array, $V_{MP-Array}$. In a system with *NP* panels and *NS*

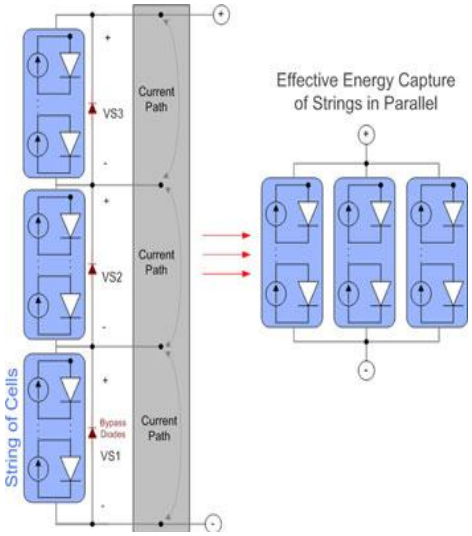

Fig.4. Conversion process forms an effective parallelization of PV strings cells per panel

Each string of cells should operate at voltage *V*String = *V*MP−Array*/NP* · *NS*. Since *V*mpp varies less with mismatch, each string of cells should operate close to its maximum power point (MPP). Fig. 5 shows the percent of maximum power achieved with the voltage equalization strategy. The *x*-axis represents the short circuit current of a string of cells, normalized to the nominal *I*SC. The curves are generated assuming the string of cells is connected in series with other strings that operate at nominal *I*SC. Perfect equalization assumes all series strings operate at identical voltages. In this case, the underperforming string operates within 99% of its MPP for over a decade of variation of *I*SC. The other curves represent the case that the voltage equalization circuit output follows a resistive load line, providing less than ideal equalization. For output resistance of 50 mΩ and a nominal *V*mpp around 15V for the string, the string operates within 98.8% of MPP for a decade of *I*SC variation. These curves reach 100% at two points because of the convex *V*mpp curve in Fig. 4. It is important to note that this does not include the power loss in the converter and only indicates relative power production of the string of cells. The dashed curve in Fig. 5 includes the effect of power loss from the 50-mΩ load line. Including resistive power loss in the balancing converter, the total power output is within 98% of MPP for *I*SC variation of a factor of 2 and90% for a decade of variation. In practice, current limits can be implemented to prevent reverse current flow into strings of PV cells which would occur in extreme shading situations as *I*SC approaches zero. Fig. 6 is a representation of a balancing converter operating in parallel with three strings of PV cells. With the converter Operating to equalize voltage across strings of cells, the converter performs an effective parallelization of the strings. This effective Parallelization provides a means to achieve the energy capture of strings connected in parallel while still achieving the higher voltage and lower copper interconnect of strings connected in Series. Major advantages of the architecture in Fig. 2 include that the each converter handles only the mismatch power, or difference in power between adjacent strings of cells. When there is no mismatch in the PV array, the converters can operate in a low power mode or turn off. In contrast with the distributed dc–dc architecture in Fig. 1(a), the full power flows through each dc–dc Converter. This means that even if there is no shading or mismatch, the insertion loss of the dc–dc converters is *PC /P*OUT or 1− *ηC*, where *P*OUT is power output from the PV module, *PC* is power loss in the converter, and *ηc* is the conversion

Efficiency of the converter. With a traditional dc–dc converter, insertion loss can be 2% or more depending on the performance of the converter and operating conditions of the panels. With the proposed architecture, insertion loss approaches the quiescent power consumption of the system that can be substantially less than 0.5% of generated PV power. For example, assuming hypothetical quiescent power is 1W (to support instrumentation and communications functions in the embedded system), for a nominal 225-W panel, insertion loss is 0.44%. To highlight the efficiency advantage of the parallel configuration, assume the efficiency as measured only by the power flow into and out of the parallel converter is 90% in a module with two strings of cells and average power per string of 100W (after mismatch is factored in). If the mismatch between adjacent strings is 10%, then the converter handles 10W to balance power flow, with total power loss of 1W. Effective conversion efficiency in this case is 99.5%.

IV. SC LADDER CONVERTER

SC circuits are effective for fixed-conversion-ratio applications as discussed in [10]–[14]. Fig. 7(a) shows a basic SC conversion cell with a 1:1 conversion ratio. Here, *VA* and *VB* are the voltages across input and output ports with power sources *V*1 and *V*2 that have series resistance *RS*. *CX* is a flying capacitance that transfers charge between *VA* and *VB*; *R*esr represents the effective series resistance (ESR) of *Cx* and switch *S*1. In the slow switching limit, the configuration of *CX* is modulated at a frequency *f*SW that is less than *either* the self-resonant frequency or ESR time constant of the loops that contain *Cbp* , *S*1, *R*esc, and *CX* [10], [11]. In phase 1, *CX* is in parallel with *VA* storing charge $QA = CX \cdot VA$. In phase 2, CX is in parallel with VB storing charge $QB = CX \cdot VB$. If *VA* > *VB*, a net current will flow from *VA*to *VB*

$$I_{DC} = \frac{VA - VB}{f_{SW} \cdot C_X} \qquad 2$$

Which can be modeled as an equivalent resistance

$$R_{eff} = \frac{1}{f_{SW} \cdot C_X}. \qquad 3$$

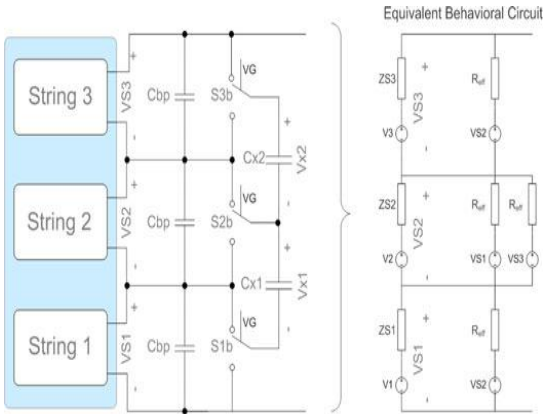

Fig. 5. SC ladder converter for balancing one PV module

Here, *R*eff is dependent only on switching frequency *f*SW, and flying capacitance *CX* and has no dependence on *R*esr. The behavioral equivalent of the circuit in Fig. 5(a) is shown in Fig. 5(b), where *R*eff is the same as in (2). Full details of the SC calculation and a comparison to the ReSC case are presented in [14]. The concept of Fig. 5(a) is extended to balance the string voltages of a PV module with the circuit represented in Fig. 6. The circuit showed in Fig. 8 implements an SC ladder converter with 1:1 conversion ratio, similar to the battery equalization circuit in [13]. Strings 1, 2, and 3 represent strings of PV cells in The circuit shown in Fig. 6 implements an SC ladder converter with 1:1 conversion ratio, similar to the battery equalization circuit in [12]. single module with voltages *VS*1, *VS*2, and *VS*3; *CX*1 and *CX*2 are

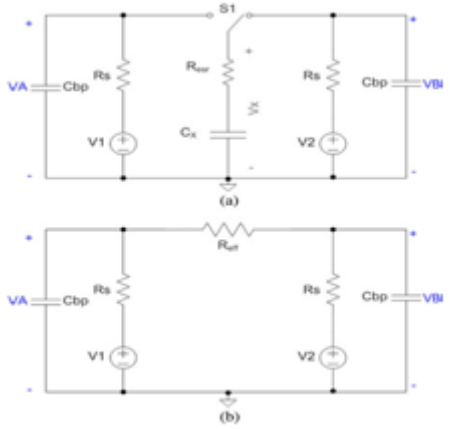

Fig.6. (a) SC conversion cell. (b) Behavioral equivalent

Flying capacitors; and *S*1*b*, *S*2*b*, and *S*3*b* represent single pole.Double -throw switches. In the behavioral equivalent, *V*1, *V*2, and *V*3 represent the open-circuit voltage of the PV strings and *ZS*1, *ZS*2, and *ZS*3 represent the nonlinear output impedance of the strings. It can be shown that as *R*eff → 0, or if *R*eff is small compared to |*ZSi*|, then string voltages *VS*1, *VS*2, and *VS*3 will be forced substantially equal. It is important to note that *R*eff is dually important parameter because it also captures power loss in the circuit—lower *R*eff improves the effective conversion efficiency of the converter.

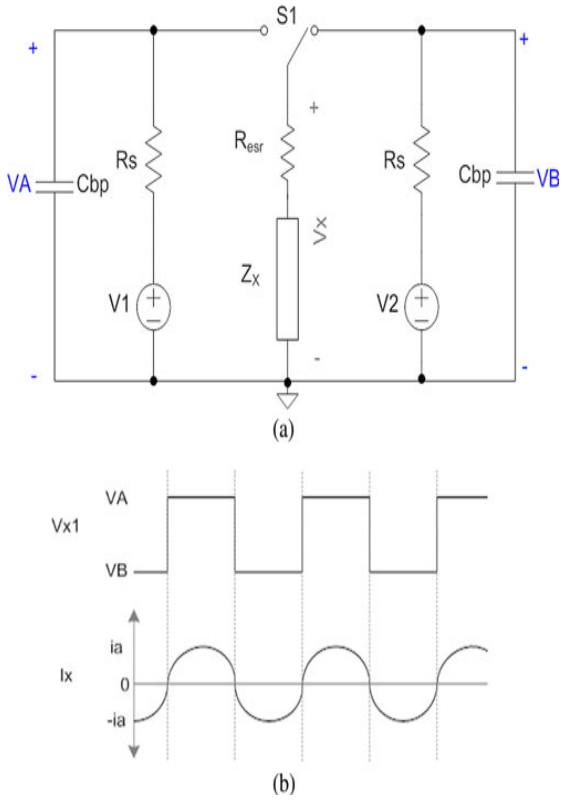

Fig. 7. (a) Resonant impedance conversion cell. (b) Current and voltage waveforms Limitations of the SC

approach include an inherent tradeoff between switching and conduction losses. This tradeoff is inherent in (2) where it is shown that *R*eff is inversely proportional to frequency. Reducing *R*eff to achieve better equalization and higher power handling is at the expense of higher switching frequency. Another limitation is the fast switching limit (FSL) that is governed by *either* the ESR time constant or self-resonant frequency of the circuit. Onset of the FSL will enforce a minimum achievable *R*eff that is dependent on *R*esr [10]. Further issues include high current spikes in the SC circuit that can complicate electromagnetic compatibility [14].

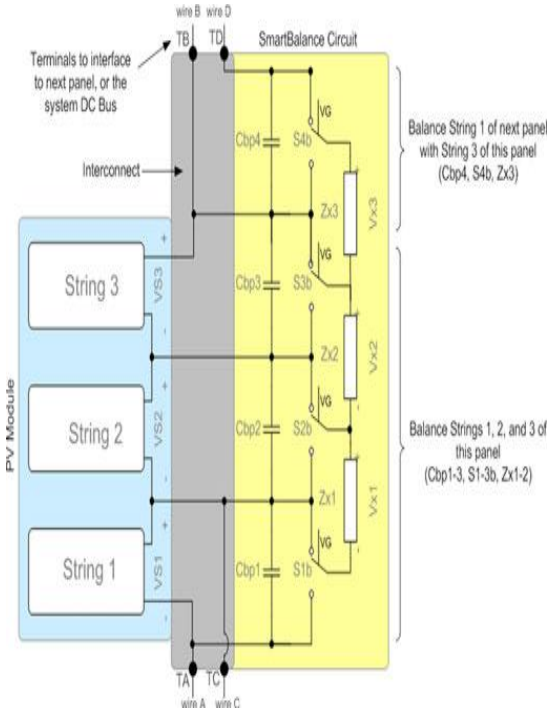

Fig. 8. Distributed converter circuit architecture

V. CIRCUIT IMPLEMENTATION

Fig. 8 shows the top-level schematic representation of the proposed converter configured with a single PV panel. Also shown is the connectivity among the panel, voltage balancing circuit, and output terminals. To extend the balancing function across a string of panels, an extra stage is added to the circuit. In this case, string-3 is balanced with string-1 of the adjacent panel. Two additional terminals are required to provide both positive

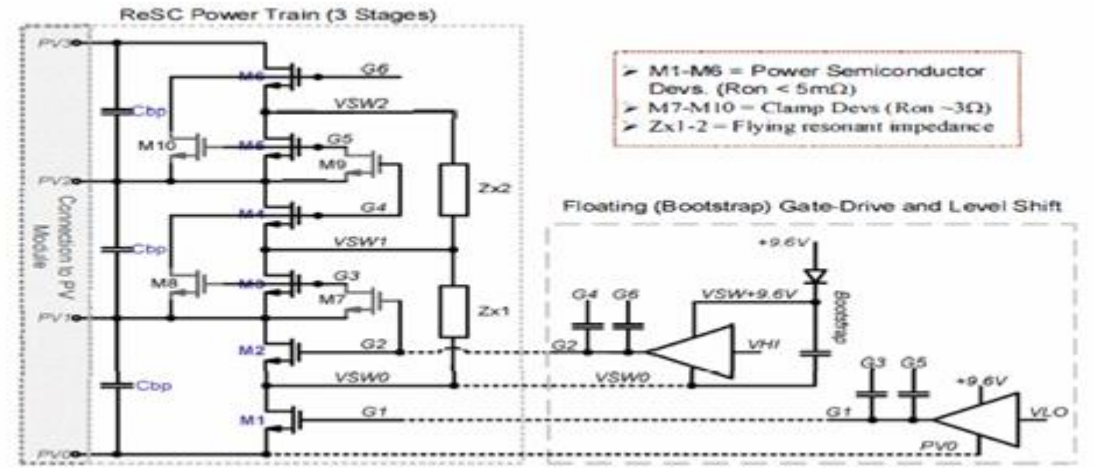

Fig. 9 Floating gate-drive and level - shift circuit for ReSc three stages of the Re-SC power train and configuration with high-voltage gate drivers

and negative voltages of string-1 of the adjacent panel. The terminals out of the package are the conventional positive and negative terminals of the PV panel (TB and TA), positiveVoltage of string-1 of the panel (TC), and a terminal to Fig. 9 Floating gate-drive and level - shift circuit for ReSc accept the positive voltage of string-1 of the adjacent panel (TD). TA and TC can be housed in the same connector out of the package or junction box. Peak current stress, and lower current harmonics. Fig. 9 shows. A low-side gate driver controls low side switches MI, M3, and M5. The ground reference for the low-side gate driver is fixed at node PVO. The high-side gate driver controls high-side switches M2, M4, and M6. The high-side gate driver is bootstrapped to the first switching node, VSWO, in order to drive the gates of the high-side switches above their respective source

terminals. Both gate drivers are coupled capacitive to higher switching nodes in the power train. To accurately tum off high voltage (floating) power devices and set the common mode for the capacitive level-shifted gate-drive signals, the power train uses clamping devices M7-MIO. Clamping devices tum on in alternate phases to directly connect the gate of higher voltage devices to the appropriate source node in the off phase. This strategy prevents unwanted tum-on of floating power devices and rapidly sets the common mode for the gate drive signals (in a single cycle).

VI. TEST RESULTS

A sub-module power management system for large-scale PV systems was presented. The advantages of a parallel-ladder architecture compared to traditional buck boost DC-DC approaches were discussed. Circuit Implementation of a resonant switched capacitor sub module prototype was presented and compared to a switched capacitor circuit alternative. Measurement results from a printed circuit board prototype based on a 0.35/lm HV-CMOS IC were discussed. The circuit achieves effective resistance significantly lower than a comparable SC converter, with insertion loss below 0.1 % and effective conversion efficiency above 99% for a wide range of mismatch. The circuit board prototype was implemented with a vertical footprint less than 6 mm, suitable for low-cost integration in the PV module junction box.

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