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Subthreshold Leakage Reduction Using Optimum Body Bias

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ABSTRACT: ***THE*** *paper consists the study of effect of source to substrate bias voltage (applied to an n-channel MOSFET and a p-channel MOSFET) on the leakage current component. The optimum value which minimizes the leakage current is found for n-MOS as well as p-MOS circuit (using simulation as well as mathematical analysis). This minimization of leakage current component eventually leads to a reduction in power dissipation (standby leakage power). On application of this leakage power reduction technique, power dissipation is reduced by about 50-70%.*

KEYWORDS: *Reverse body bias, subthreshold leakage, optimum value, body effect, weak inversion.*

I. INTRODUCTION

The increasing prominence of portable systems and the need to limit power consumption in very high density VLSI chips have led to rapid and innovative developments in low power design during the recent years. The driving forces behind these developments are portable device applications requiring low power dissipation, high speed and high throughput. Hence, low power design of digital integrated circuits has emerged as a very active and rapidly developing field.

Here, the technique used to achieve low power consumption in digital systems emphasizes on the application of an optimum value of reverse body bias which helps to reduce leakage power consumption in digital circuits [9].

II. SOURCES OF POWER DISSIPATION

The total power dissipation consists of two components:

(a) Static power dissipation, due to a leakage current of transistors during steady state.

(b)The dynamic power dissipation, which has two components: short circuit power dissipation and power dissipation due to charging/discharging of node capacitance.

In many new high performance designs, the leakage component of power consumption is comparable to the switching component. This percentage increases with technology scaling. This paper discusses a technique to bring leakage under control.

The four main sources of leakage current in a CMOS transistor are: Reverse-biased junction leakage current (I_{REV}), Gate induced drain leakage (*GIDL*), Gate direct-tunneling leakage (I_G) and Subthreshold (weak inversion) leakage (I_{SUB}). In current CMOS technologies, the subthreshold leakage current, I_{SUB}, is much larger than the other leakage current components [10].

III. EFFECT OF REVERSE BODY BIAS ON SUBTHRESHOLD LEAKAGE

The subthreshold leakage is the drain-source current of a transistor operating in the weak inversion region. Unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device.

The body effect causes an increase in V_T as the body of the transistor is reverse-biased (i.e., V_{SB} of an NMOS transistor is increased) [2].

$V_T = V_{T0} + \gamma (\sqrt{(|2\Phi_F| + V_{SB})} - \sqrt{|2\Phi_F|})$ (Eqn.-1)

where V_T = Transistor threshold voltage with source to substrate voltage (V_{SB})applied, V_{T0} = Threshold voltage when $V_{SB} = 0$, Φ_F =substrate Fermi potential, γ = substrate bias coefficient [4].

Also, I_{SUB} is directly proportional to e^{-V_T}. Hence, decreasing the threshold voltage increases the leakage current exponentially [5].

IV. DETERMINATION OF OPTIMUM REVERSE BIAS

When a positive substrate voltage is applied to the p-MOS substrate, the power dissipation first decreases upto some value of V_{bs} and then it starts to rise (Fig,1). This value (which is 3.6 V in this case-Simulation is done using 180 nm technology at supply voltage, V_{dd}=1.8V) of V_{bs} gives the optimum RBB value for p-MOS. But the supply voltage available is 1.8V. So, the optimum V_{bs} value is chosen as 1.8V (instead of 3.6V).

Similarly, when a negative voltage is applied to n-MOS substrate, as the value of V_{bs} becomes more negative, power dissipation decreases and becomes minimum at V_{bs}= -0.6V(Fig. 2). A further decrease of V_{bs} leads to an increase in power dissipation.This gives optimum value of RBB for n-MOS.

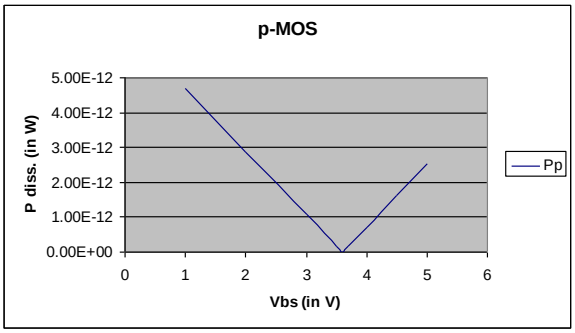

Fig. 1 Power dissipation as a function of substrate to source voltage applied (for p-MOS)

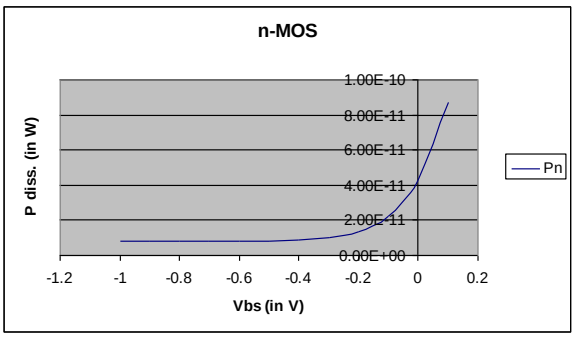

Fig. 2 Power dissipation as a function of substrate to source voltage applied (for n-MOS)

Mathematical analysis shows that for n-MOS device $V_B > 0.72$ V and for p-MOS device $V_B < 2.52$ V (inorder to make value of V_T in Eqn.-1 real)

V. LEAKAGE CONTROL IN LOGIC GATES

The standard logic gates show a decrease in standby power dissipation when the optimized reverse body bias is applied to substrate. A comparison of this is shown in Fig. 3,4,5,6 for various input combinations for 2-input NAND, AND, NOR and OR gates respectively. Here, P1=Power dissipation when V_{bs} =0V (no substrate bias applied) and P2= Power dissipation when V_{bs} is applied (1.8V for p-MOS and -0.6 V for n-MOS).

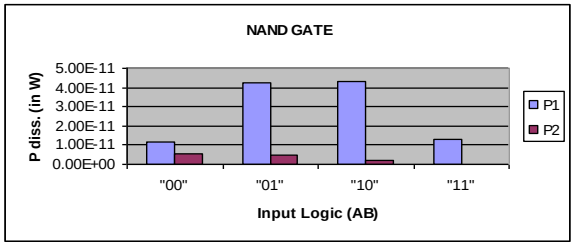

Fig. 3 Power dissipation with and without RBB for various input combinations for 2-input NAND gate

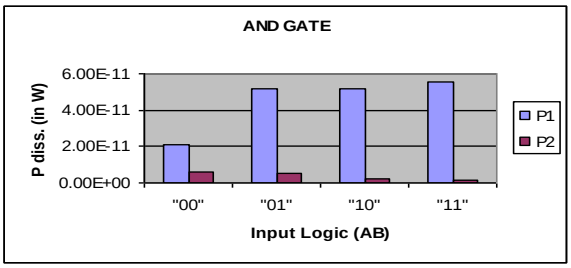

Fig. 4 Power dissipation with and without RBB for various input combinations for 2-input AND gate

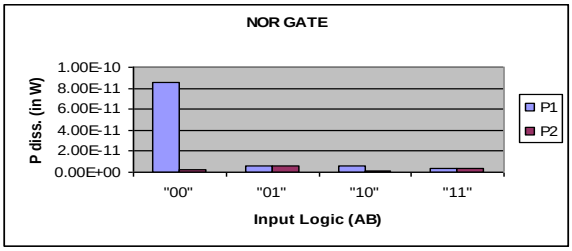

Fig. 5 Power dissipation with and without RBB for various input combinations for 2-input NOR gate

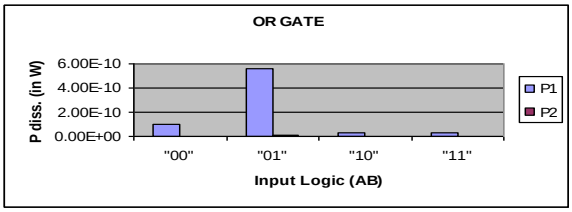

Fig. 6 Power dissipation with and without RBB for various input combinations for 2-input OR gate

For a CMOS inverter the variation of V_T when V_{BS} is varied is shown in Table 1. When RBB is applied, V_T value increases.

TABLE 1. THRESHOLD VOLTAGE OF INVERTER WITH AND WITHOUT RBB

V_{BS}	V_T (by simulation)	V_T (mathematically)
0V	0.74 V	0.694 V
Applied	0.82 V	0.81 V

VI. CONCLUSION

We demonstrated that the power dissipation reduced by about 50-70% on application of reverse body bias voltage (optimum value found). The values of Optimum Reverse Body Bias were calculated mathematically as well as using simulation method. We used SPICE circuit simulator and 180 nm technology to arrive at above results. However this technique usually requires twin-well or triple-well CMOS technology to apply different substrate bias voltages to different parts of the chip.

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